The Examiner's reconsideration is respectfully requested as the circuit disclosed in Denki is not as described in the Action and as relied upon by the Examiner in forming his rejections. In general, Denki discloses a well known circuit that has been used in many types of linear DC regulators. A zener diode is always used as a reference voltage, fed by a resistor or constant current source, having a capacitance across the zener diode as noise filter and/or inrush control. The choice of capacitance determines the degree of inrush control versus output filter size. Real voltage regulator circuits always include active current limit means that both preserve the output pass device but also make inrush control circuits unnecessary.

Relative to claim 1, it contains the following limitations:

> Transistor means electronically connected to said operational amplifier circuit, said transistor means operating in a linear mode during capacitor charging, and subsequently reaching a full-ON state;
>
> Energy storage load means connected to said transistor means for receiving a full power supply after said transistor means reaches its full-ON state.

The transistor of Denki, by contrast, can never reach a full-ON state. The principal object of Denki is to serve as a "constant voltage power supply." The output transistor, whether a FET or BJT, is <u>always</u> linear in operation, and can never reach a full-ON state. As such, a voltage reference ZD1 is required, and operation of the whole circuit is considerably different that the presently claimed circuit.

In addition, Denki is truly not relevant (analogous) prior art. As described above, the Denki circuit was designed to perform a completely different function from that being performed by the present invention. The engineering problem being addressed in Denki is entirely different from the engineering problem being solved by the present invention, and one skilled in the art would not look to Denki when trying to solve the problem associated with the instant invention. As such, under the test set forth in Wang and discussed in the response filed April 9, 2002, Denki is not analogous prior art.

Relative to claim 6, as discussed above, Denki is never in a full-ON state. Constant output voltage DC supplies operate in linear modes at all times, except when disabled by a control input signal (full-OFF), but are never full-ON. As such, the limitation of claim 6 cannot be anticipated by Denki.

Relative to claims 17 and 18, the Examiner's interpretation of the X1 device being a delay element is incorrect per the patent text (see Paragraph 0033) which plainly identifies it as a "constant current element X1." This is an alternate and preferred way to bias zener diodes, and has been in common use since the invention of the zener diode. The primary reason to use constant current source is to improve line regulation since zener current does not change with input voltage as it would with a resistor. It has essentially nothing to do with ramp-shaping since a resistor in its place would produce a decent ramp in the early part of its exponential rise. The subject invention does not include a constant current source, but achieves the desired ramp shape by using a truncated exponential rise from the R-C elements, which is far simpler and less expensive.

Relative to claims 7 and 8 and the Kajimoto reference in particular, Kajimoto is non-analogous art, or is at least not relevant in forming the basis of a 103 rejection as it is solving a problem not anticipated by the present invention. Kajimoto shows a capacitor connected across two leads of the output device, but for an entirely different purpose that the present invention. Kajimoto's capacitor 12 is applied from Gate to Drain, and for purposes of reducing output transients when the circuit is required charge depleted capacitive load memory cells, enhancing the Miller effect inherent in the PFET device to the benefit of circuit stability. It forms a low impedance negative feedback path for high frequencies only, while the op-amp takes care of slower phenomena and DC regulation. The subject invention utilizes a small capacitor applied from Gate to Source merely to guarantee an OFF state for the PFET at the instant of power-on while the op-amp output is observed to be rising at its typical .5V/us slew rate to reach the point at which the feedback loop is stable with the PFET device still OFF, but the circuit is then ready to perform according to the rules governing op-amps. To anyone skilled in the art, the present invention and Kajimoto are dealing with entirely different and unrelated design challenges with clearly different solutions.

As this response is in support of a Request for Continued Examination under 37 CFR 1.1114, a check in the amount of $1680 to cover the RCE filing fee and the Petition for a Three Month Extension of time, submitted herewith, is enclosed.

In view of the foregoing remarks, the Examiner's reconsideration is respectfully requested.

Respectfully submitted

Date: 5/19/03

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